Refine Search

Your wildcard search against 10000 terms has yielded the results below.

Your result set for the last L# is incomplete.

The probable cause is use of unlimited truncation. Revise your search strategy to use limited truncation.

Search Results -

Terms	Documents
L11 and bit$ and (error$ or signal$ or except$)	35

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L12

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Thursday, December 09, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=ADJ			
L12	L11 and bit$ and (error$ or signal$ or except$)	35	L12
L11	L10 and switch$	35	L11
L10	l3 and branch$ and pipe$	35	L10
DB=TDBD; PLUR=YES; OP=ADJ			
L9	cpu and process and execut$ and register and stack and virtual and overflow and underflow program counter and variable$ and accelerat$	0	L9
DB=DWPI; PLUR=YES; OP=ADJ			
L8	cpu and process and execut$ and register and stack and virtual and overflow and underflow program counter and variable$ and accelerat$	0	L8
DB=JPAB; PLUR=YES; OP=ADJ			

L7	cpu and process and execut$ and register and stack and virtual and overflow and underflow program counter and variable$ and accelerat$	0	L7
DB=EPAB; PLUR=YES; OP=ADJ			
L6	cpu and process and execut$ and register and stack and virtual and overflow and underflow program counter and variable$ and accelerat$	0	L6
DB=USOC; PLUR=YES; OP=ADJ			
L5	cpu and process and execut$ and register and stack and virtual and overflow and underflow program counter and variable$ and accelerat$	0	L5
DB=PGPB; PLUR=YES; OP=ADJ			
L4	cpu and process and execut$ and register and stack and virtual and overflow and underflow program counter and variable$ and accelerat$	0	L4
DB=USPT; PLUR=YES; OP=ADJ			
L3	L2 and accelerat$	36	L3
L2	L1 and program counter and variable$	110	L2
L1	cpu and process and execut$ and register and stack and virtual and overflow and underflow	236	L1

END OF SEARCH HISTORY

Terms used
virtual and **execute** and **cpu** and **overflow** and **underflow** and **operand** and **move** and **register** and **memory**

Sort results by relevance

Display results expanded form

Save results to a Binder

Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Best 200 shown

Relevance scale

1 The KScalar simulator

J. C. Moure, Dolores I. Rexachs, Emilio Luque

March 2002 **Journal on Educational Resources in Computing (JERIC)**, Volume 2 Issue 1

Full text available: pdf(493.35 KB) Additional Information: full citation, abstract, references, index terms

Modern processors increase their performance with complex microarchitectural mechanisms, whicl makes them more and more difficult to understand and evaluate. KScalar is a graphical simulation tool that facilitates the study of such processors. It allows students to analyze the performance behavior of a wide range of processor microarchitectures: from a very simple in-order, scalar pipeline, to a detailed out-of-order, superscalar pipeline with non-blocking caches, speculative execution, and comp ...

Keywords: Education, pipelined processor simulator

2 The Clipper processor: instruction set architecture and implementation

W. Hollingsworth, H. Sachs, A. J. Smith

February 1989 **Communications of the ACM**, Volume 32 Issue 2

Full text available: pdf(4.67 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Intergraph's CLIPPER microprocessor is a high performance, three chip module that implements a new instruction set architecture designed for convenient programmability, broad functionality, and easy future expansion.

3 An example RISC vector machine architecture

Martin Dowd

September 1987 **ACM SIGARCH Computer Architecture News**, Volume 15 Issue 4

Full text available: pdf(484.57 KB) Additional Information: full citation, index terms

4 A VLIW architecture for a trace scheduling compiler

Robert P. Colwell, Robert P. Nix, John J. O'Donnell, David B. Papworth, Paul K. Rodman

October 1987 **Proceedings of the second international conference on Architectual support fo programming languages and operating systems**, Volume 15 , 22 , 21 Issue 5 , 10 , 4

Your search matched **0** of **1099723** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

overflow and underflow and virtual and acclerator ar Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

Results:
No documents matched your query.

Refine Search

Search Results -

Terms	Documents
(712/244 |712/210).ccls.	756

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Thursday, December 09, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=ADJ			
L4	712/244,210.ccls.	756	L4
L3	717/147,148,149.ccls.	297	L3
L2	717/143.ccls.	168	L2
L1	717134,135,136,137,138,139,140.ccls.	0	L1

END OF SEARCH HISTORY